**ECE 324 Homework6: FSM design and simulation**

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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| **Exercise** | **Course outcome** | | **Grade** |
| Homework6 | | 2.a, 7.b | /30 |

2.a. Define engineering problems from specified needs for digital systems including implementation on FPGAs using HDL programming.

7.b. Employ appropriate learning strategies such as communicating with an expert, using external resources, experimentation, simulation, etc.

# Learning Objectives

1. Learn SystemVerilog coding techniques for FSM design.
2. Use logic simulation to verify functional correctness of an FSM.

# Exercise

1. Complete the state machine in CoinDetector.sv as specified in Lecture7.
2. Write a testbench for the Coin Detector. To produce a reasonable simulation time and display, set the parameters during the module instantiation to the following:  
   dimeMin = 2  
   dimeMax = 4  
   nickelMin = 6  
   nickelMax = 8  
   quarterMin = 10  
   quarterMax = 12  
   The testbench must generate a clock and verify all state machine transitions. Include comments in the testbench that explain what is being tested. Also include assertions to verify when the coin detect outputs should be on and off.
3. Simulate using Vivado.
4. Submit to Blackboard your state machine, testbench, screenshot(s) of your simulation results (make sure that signal name and time labels are legible), and a written report (with cover sheet) that explains how your simulation results prove that the FSM functions correctly.